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Application Note

SCANNING LOGIC FOR RF SCANNER-RECEIVERS USING CMOS INTEGRATED CIRCUITS

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This note describes the application of CMOS integrated logic circuits in R.F. scanner-receiver control functions. Approaches considered include crystal switching methods with and without priority channel capability, of both the fixed and selectable priority channel types, along with reference to their applicability in phase-locked loop system designs.

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INTRODUCTION

This application note describes various methods of implementing the contorl functions necessary in R.F. scanner receiver sets. The basic function of a scanner receiver is outlined, followed by various methods of performing the scanner functions with standard CMOS logic integrated circuits. The various control functions described range in complexity from simple methods of crystal switching and priority channel monitoring to more sophisticated techniques incorporating phase-locked loop receiver designs.

SCANNER RECEIVER CHARACTERISTICS

In public communications work it is often necessary or desirable to monitor several channels of interest so that cognizance of all important activity can be maintained. Radio-frequency scanner-receivers are the tools with which the task is most often accomplished.

R.F. scanner-receivers are electronic systems designed to sequentially sample several communications channels within a given radio frequency band, and automatically lock onto a channel that is active during the sample period. Typical bands of operation include LVHF (≃30-50 MHz), HVHF (≃145-175 MHz), UHF (≃440-470 MHz), etc. Users of scanner-receivers range from public service personnel, such as policemen or utility maintenance people, to the hobbyist.

An R.F. scanner receiver may be broken down into the following functional blocks as seen in Figure 1: receiver "front-end", mixer, intermediate frequency amplifier, demodulator, squelch control, scanning logic, local oscillator, and audio output.

The I.F. signal is demodulated to produce the audio signal. This demodulator output can also be used to activate or deactivate the squelch. The squelch circuit is essentially a detector used to discriminate between signal and noise. This circuit typically provides a dc bias or AGC signal to the audio output stage to prevent noise from passing through while the channel is not active. When the channel being sampled is active, the squelch changes state and the resulting signal is used to activate the audio stage and to inhibit further scanning. Thus the receiver remains on the channel until the squelch signal goes away (indicating a secession of activity on the given channel). Normally, a delay network is designed into the squelch circuit such that the appearance of an I.F. signal will cause an immediate reaction, but reaction to the disappearance of an I.F.signal is delayed some finite period of time to prevent leaving a channel prematurely in the event that communication is momentarily interrupted (i.e., while going under a bridge, etc.). Figure 2 shows the block diagram of a typical squelch circuit. Finally, the scanning logic is that part of the circuit that sequentially selects the desired channel frequencies and automatically locks the system on to an active channel under control of the squelch. It is the scanning logic portion of R.F. scanner-receiver systems to which this paper is addressed.

There are two basic approaches to be considered. The

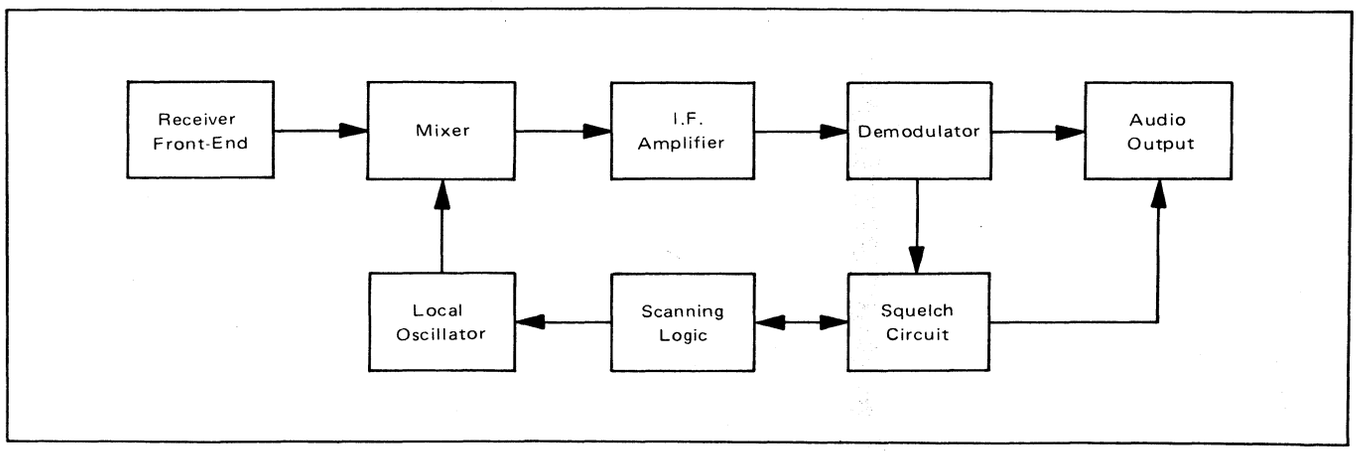

FIGURE 1 – Scanner Receiver Functions

first, and most widely used by present manufacturers, is the "crystal switching method." This method employs a single standard oscillator into which different crystals (representing different channels) are switched. The second and more sophisticated approach involves the utilization of a phase-locked loop. There is a third category of scanner receivers which, while utilizing either one of the two aforementioned approaches, offers the additional capability of continuously sampling a channel of "high priority" whether or not activity is present on any other channel. Either one of the basic approaches, with or without priority channel monitoring capability, may be implemented efficiently with CMOS integrated circuits.

the Clock (C) input, providing the Clock Enable (CE) input is low. The squelch signal controls the CE input. When there is activity on a selected channel, the squelch signal goes high and inhibits the Johnson counter from advancing to the next channel.

The crystal interface drivers are composed of two MC75492 drivers, each being a package of six interface inverters. Each inverter is a bipolar NPN Darlington transistor in a common emitter configuration with an open collector output. The base circuitry contains sufficient series resistance to allow direct interfacing with the CMOS driving logic. When an inverter is turned on by the Johnson counter, its output goes low, thus forward biasing

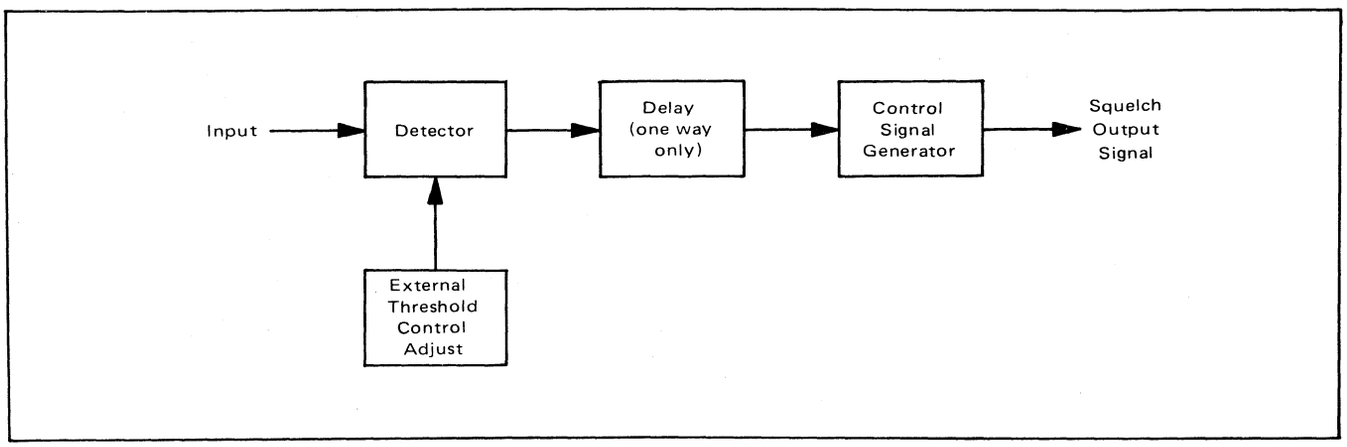

FIGURE 2 – Block Diagram of Typical Squelch

CRYSTAL SWITCHING

Fundamentally, the crystal switching method can be divided into three sections: a control section, a sequencer, and the crystal interface drivers. Present manufacturing methods utilize discrete components, discrete gates, and individual gate packages for the required functions. Alternate approaches, such as those about to be described, can prove to offer substantial improvement in simplification and efficiency.

The logic for the basic scanner function is shown in Figure 3. The control section is composed of two CMOS clocks and the squelch signal. Clock A is designed to free run at approximately 15 Hz, and is used for normal scanning. Clock B is designed to oscillate at approximately 1.5 Hz and is gated such that it will only oscillate when switch SW2 is set to ground. This clock is used for manual stepping. Switch SW1 is used to select between the manual and the scan modes. The third part of the control section, the squelch signal, must switch between appropriate logic levels (i.e., ground and V_{DD}), where a logic "high" corresponds to activity being present on the particular channel being sampled.

The sequencer function is accomplished by a MC14017 Johnson counter. The ten outputs are normally low and go high only at their appropriate time period. The output changes occur sequentially with each positive transition of

the LED and the PIN diode which enables the associated crystal in the oscillator circuit. The MLED 650 is a panel mount visible red light emitting diode used ot indicate the channel being monitored. The LED current is determined by resistors R1 and R2. The MPN3401 (or MPN3402) shown in Figure 3 is a silicon PIN diode designed for R.F. switching applications. When the PIN diode is forward biased, the extremely low ON-impedance provides the "AC ground" signal path for the crystal in the oscillator circuit. The bias current for the PIN diode is set by resistor R2. The inductor provides decoupling and isolates the Darlington drivers from the oscillator resonant circuit. When the inverter is off, R1 acts as a pull-up resistor to insure that the PIN diode is off, preventing the corresponding crystal from interacting with others. Note that single pole switches may be placed as shown in the schematic, in series between the drivers and LEDs, allowing the user to "lock-out" any channel that is not to be scanned.

CMOS integrated circuits are ideal for the control and sequencer sections because of the simplicity of design, low power consumption, and versatility in power supply requirements. Because CMOS logic will operate with a supply voltage in the range of 3 to 16 volts, the need for a separate +5.0 volts logic power supply is eliminated and the logic may be powered by the existing receiver power supply.

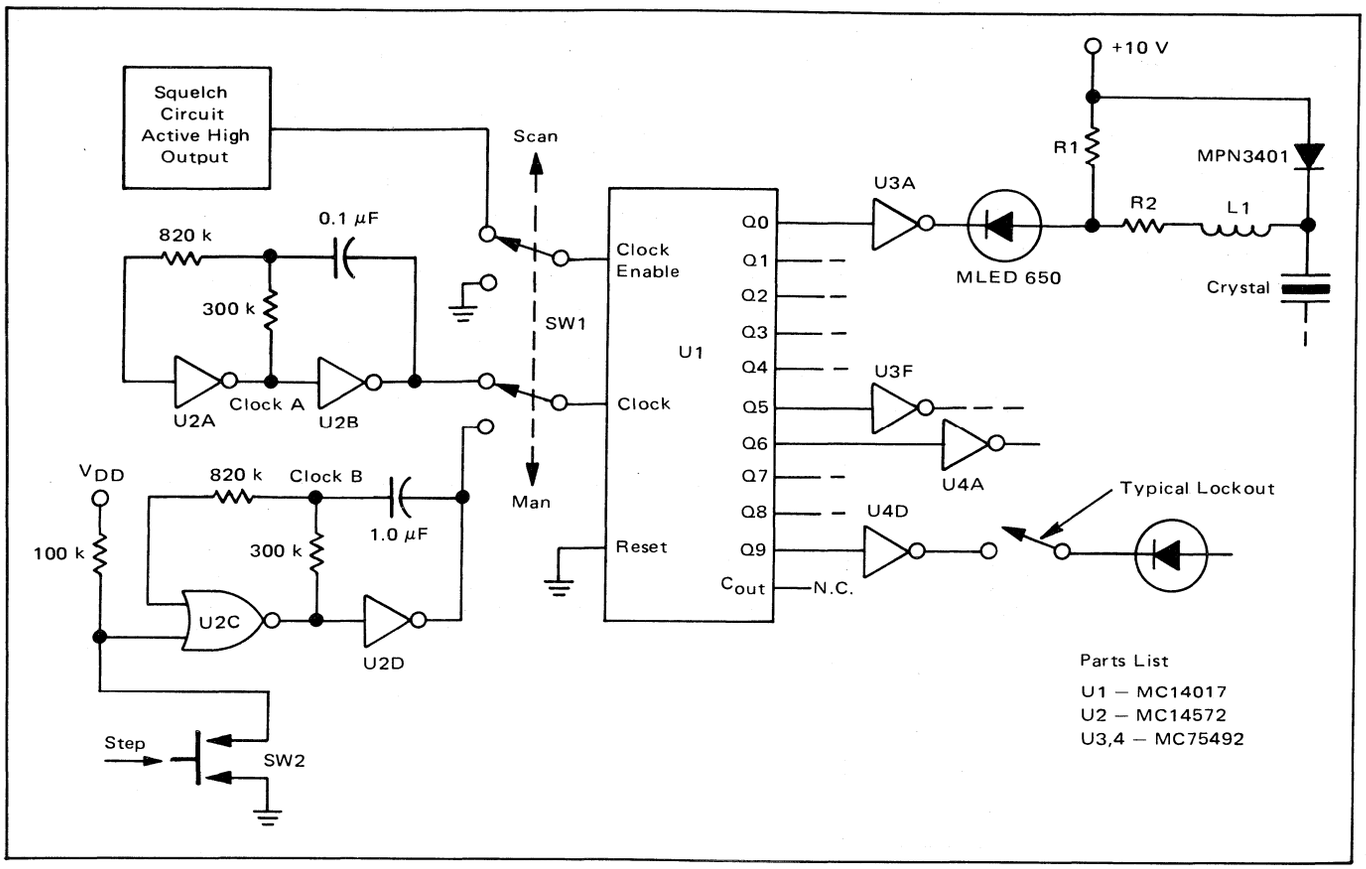

FIGURE 3 – Basic Scanner Logic (10-Channels)

PRIORITY CHANNEL MONITORING

The next step up in a scanner-receiver is the addition of a "priority channel." Such an addition allows the user to designate a particular channel frequency as being of high priority. The scanner logic will automatically sample this priority channel at a fixed rate. Should the priority channel be active during the sampling interval, the receiver will switch to the priority channel even though it may have been locked to another active frequency. The priority channel monitoring feature finds great usefulness in the public service communications field. There are two types of priority mechanisms to consider: the selectable, and the fixed priority channel shown in Figure 4.

In the control section, the Clock A circuit is the same as that previously discussed in the basic scanner design, switch SW1 is still used to choose between the manual and automatic scanning mode of operation, and switch SW2 is still used to enable manual "step" clocking. The Clock B oscillator has been altered to have an output as shown in Figure 5. The positive output pulses are now approximately 10 ms in width with a repetition rate of 1.5 Hz. Clock B is still used for manual stepping, but now also controls the sampling of the priority channel. Added to the control section is the priority response circuit, composed of a NAND gate, an inverter, and two R-C delay networks. The sequencing function is still performed by clocking a CMOS Johnson counter.

The crystal interface drivers are now three MC75491s, each being a package of four inverters. The MC75491 differs from the MC75492 specified previously in that each inverter has both an open collector and open emitter outputs. Each inverter is still, however, an NPN Darlington transistor with a series base resistor network. The emitters of all the inverters of the main crystal bank are tied to the collector of another single inverter, U5B, whose emitter is then grounded. When the inverter is on, the emitters of the other inverters are brought to ground, thus allowing the normal scanning operation. When inverter U5B is off, the emitters of the other drivers and the associated crystals are disabled. Simultaneously to U5B switching off, driver U5D is switched on enabling the priority channel crystal. Note that the priority channel is not scanned as a part of the main crystal bank and is separately controlled. To change the priority channel frequency requires a replacement of the channel crystal.

Operation of the fixed priority channel circuit (Figure 4) is illustrated by the timing diagram in Figure 5.

Clock B is used to turn off the main crystal bank, and simultaneously turn on the priority channel, for approximately 10 ms. When this happens, the NAND gate, U2E, of the priority response circuit is enabled after a six millisecond R-C delay and interrogates the level of the squelch signal. The purpose of the delayed enable is to allow the receiver to settle out, prior to sampling the squelch. The

output of inverter U2F is basically the AND function of the interrupt clock and the squelch signal. A high level would indicate activity on the priority channel. This signal is then fed through the priority mode switch SW3 to inhibit the clock locking the system to the priority channel.

The priority channel will remain locked in until activity disappears, the squelch signal dies, and the output of the priority response circuit again goes low. Note, however, that the R-C delay between gates U2E and U2F prevents the priority response circuit from reacting to the disappearance of a squelch signal for roughly 50 ms. This prevents the system from reacting prematurely to temporary interruptions of priority activity. Upon disappearance of priority activity for longer than the delay time, the system would once again be set into a scan mode. Note also that the priority channel sampling is active both if the system is scanning or if it is locked onto another channel – a continuous watch is kept over the priority channel. If the user does not wish to be switched over automatically to the priority channel when it is active, but wishes only to be alerted when activity is present, then priority mode switch SW3 would be set to the "blink" position. This will allow Clock B to free run and a LED driven by U5C will then blink indicating the presence of priority activity but no changeover will occur. The priority channel can again be activated by returning the priority mode switch SW3 back to the "Auto" position.

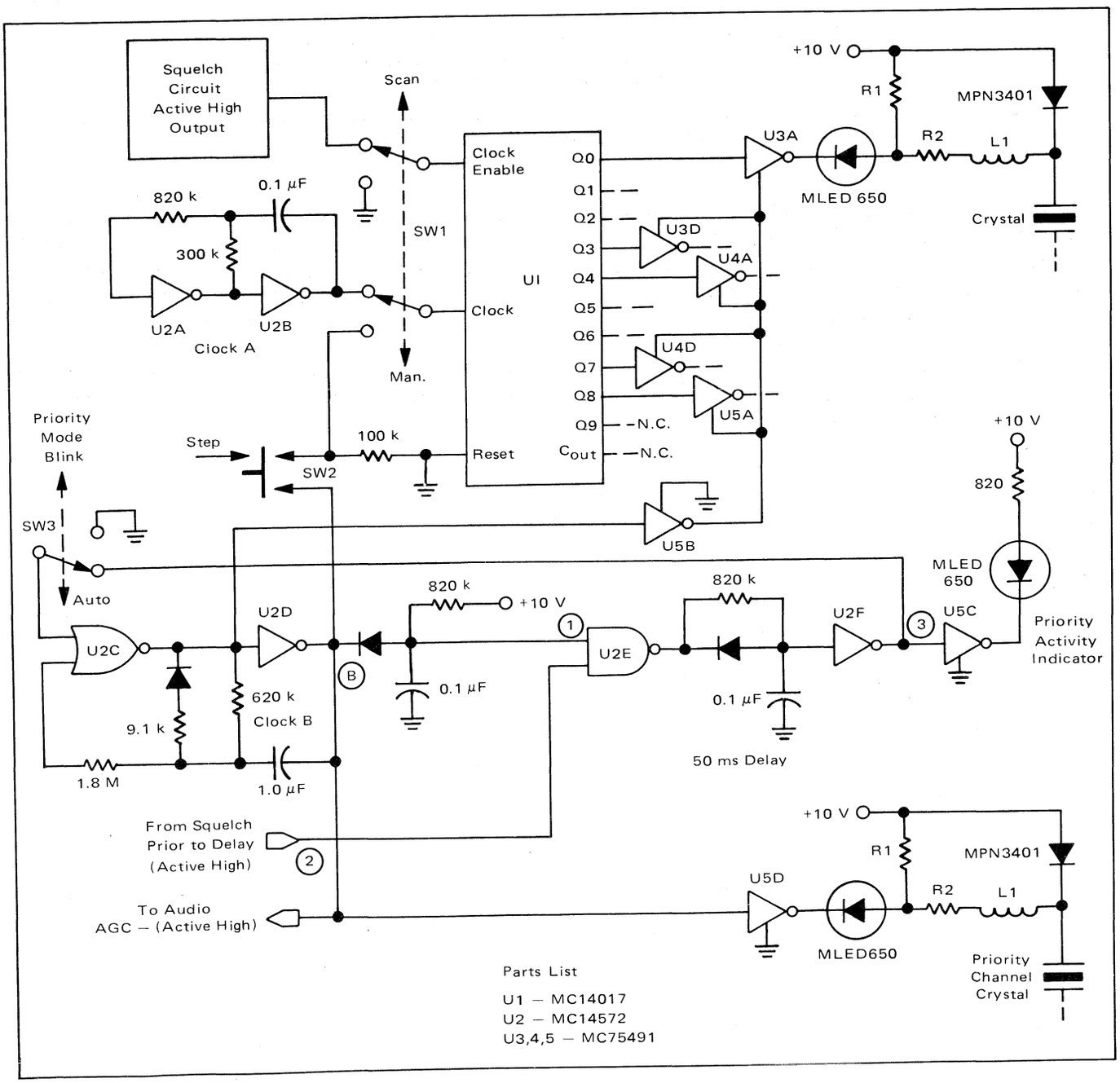

FIGURE 4 – Fixed Priority Channel Logic (9-Channels Plus Priority)

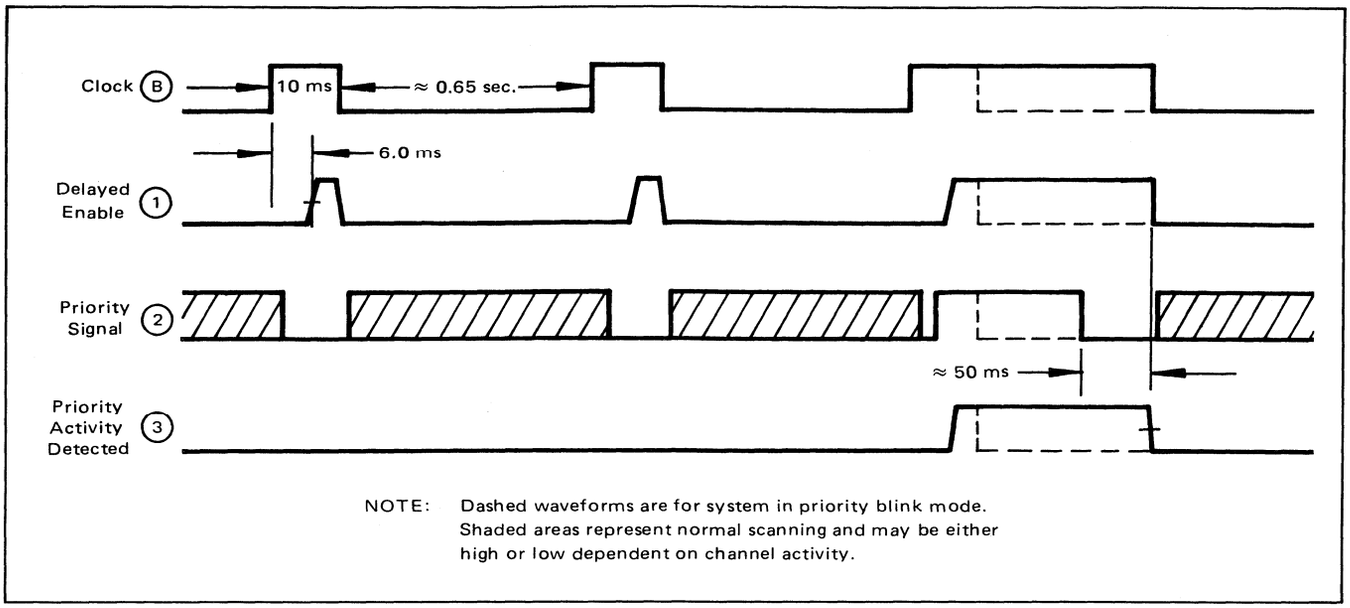

FIGURE 5 – Scanner Logic Priority Timing

Figures 6 and 7 illustrate two different approaches to achieving a selectable priority function. Figure 6 is a modification of Figure 4, and operates principally the same way as the fixed priority channel mechanism. A rotary switch performs a collector wired – OR connection of the priority channel driver U5D to achieve the selectability. This allows the user to change the priority channels without physically interchanging the crystals.

Figure 7 illustrates a slightly more sophisticated approach. The control section is essentially the same as those previously described, with the exception that Clock B is permitted to free run. The sequencer section of the circuit is changed somewhat from previous designs. A binary coded thumbwheel switch is used to select the priority cahnnel. The encoded channel number is applied to the preset inputs of MC14510, BCD presettable counter, and to the Y inputs of the MC14519, quad two channel data selector. The Q outputs of the MC14510 counter are the X inputs of the data selector. The sequencing Clock A advances the MC14510 with each positive transition and the squelch signal applied to the Carry In input provides the "clock inhibit" function. The MC14028, BCD to one-of-ten decoder, converts the BCD code present at the Z outputs of the data selector to its decimal equivalent, subsequently turning on the corresponding crystal driver. With the A and B control inputs to the MC14519 high and low respectively, data at the X inputs is present at the Z outputs. Thus, manual and automatic clocking of the MC14510 counter results in stepping sequentially through the various channels. However, with B high and A low, the data that is present at the Y inputs is transferred to the Z outputs. Subsequently, the channel crystal that is enabled corresponds to the particular setting of the thumbwheel switch.

With the thumbwheel switch used to select the priority channel, priority channel sampling is achieved by switching the A and B inputs of the MC14519 for roughly a 10 ms period. As previously discussed, the squelch is sampled after a finite delay time to determine the status of the priority channel. A high signal indicating activity is used to preset the MC14510 counter with the priority channel code. The BCD representation of the priority channel will thus be present at the Q outputs of the MC14510, and the X inputs of the MC14519. When the control inputs A and B of the MC14519 switch back again, the priority channel code will remain at the input of the MC14028 decoder.

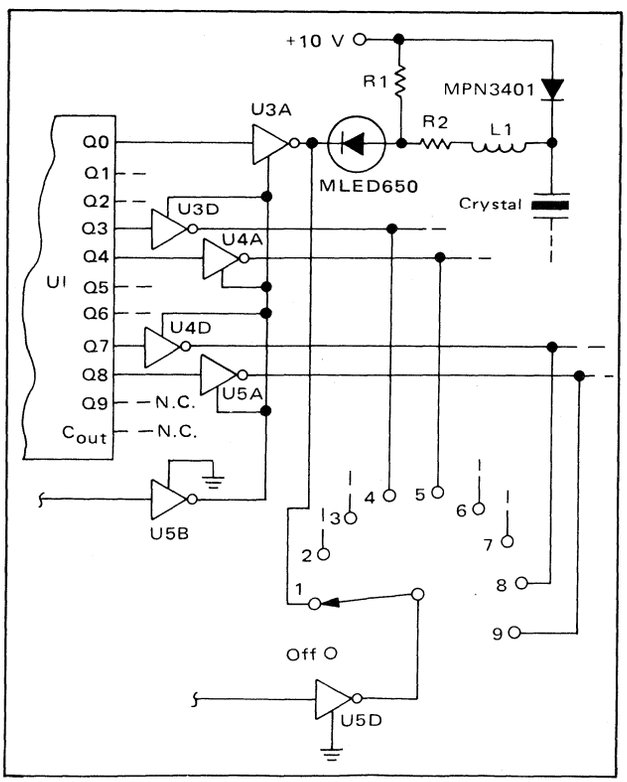

FIGURE 6 – Selectable Priority (9-Channels)

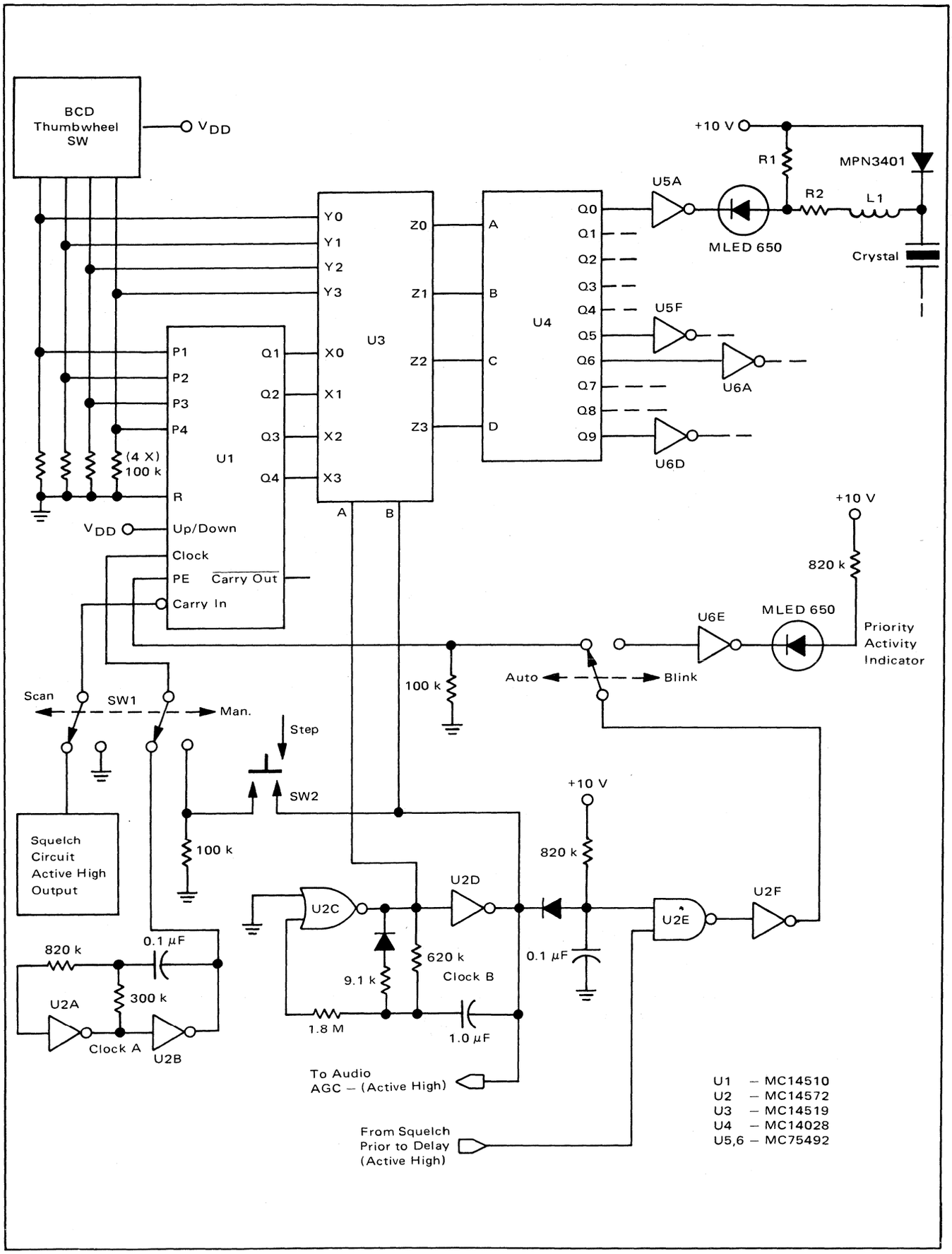

FIGURE 7 – Thumbwheel Programmable Priority (10-Channels)

The clocking of the MC14510 will continue to be inhibited since the squelch signal remains high while there is activity on the channel. If no activity is present on the priority channel during the sample period, no change in the outputs of the MC14510 is effected and the circuit remains in its previous mode of operation. Note that approximately a 6.0 ms delay to allow system settling at the beginning of the sampling period is still incorporated, however, a separate priority channel delay, to prevent leaving the priority channel prematurely, is no longer needed. Presetting the priority code into the MC14510 (upon detection of priority activity) automatically activates the normal squelch delay for that purpose.

APPLICATION IN PHASE-LOCKED LOOP DESIGNS

Much of the same control logic described for the crystal switching methods may also be applied in a phase-locked loop design. The major advantages of a phase-locked loop system are, of course, that a crystal for every channel is no longer needed, and, depending upon the design of the loop and the receiver front-end, the number of channels that may be scanned is significantly greater.

The basic approach to a scanning logic design for a phase-locked loop system is illustrated in Figure 8. The user would program into a memory system the frequencies that he wishes to scan within a given band. The programming-memory section would be one that would input and store in the memory block the proper values of N, corresponding to the desired frequencies, to be used in the divide-by-N part of the loop (the outputs of the memory would interface directly with that part of the loop). The control block would then be used to address the memory, either with the outputs of the Johnson counter, or with the BCD outputs of the MC14519 or MC14510 shown in Figure 8 (depending upon the type of addressing required). The memory block could be filled by any type of static or dynamic memory system that was found suitable.

SUMMARY

Standard CMOS integrated logic circuits can effectively be used to accomplish the control functions of R.F. scanner-receivers. Illustrated and described in this application note were methods of implementing scanning logic for crystal switching receiver sets, with or without fixed or selectable priority channel capability. It was pointed out that the logic circuits as described could also effectively interface with phase-locked loop system designs.

CMOS integrated logic circuits are ideally suited for use in R.F. scanner receivers due to their low power dissipation, high noise immunity, and applicability over a wide range of power supply voltages. With the use of CMOS, both digital and analog functions may be operated from the same supply. Finally, with the high density capability of CMOS technology, the various control and sequencing functions described could perhaps be integrated onto a single chip, further reducing the cost and package count.

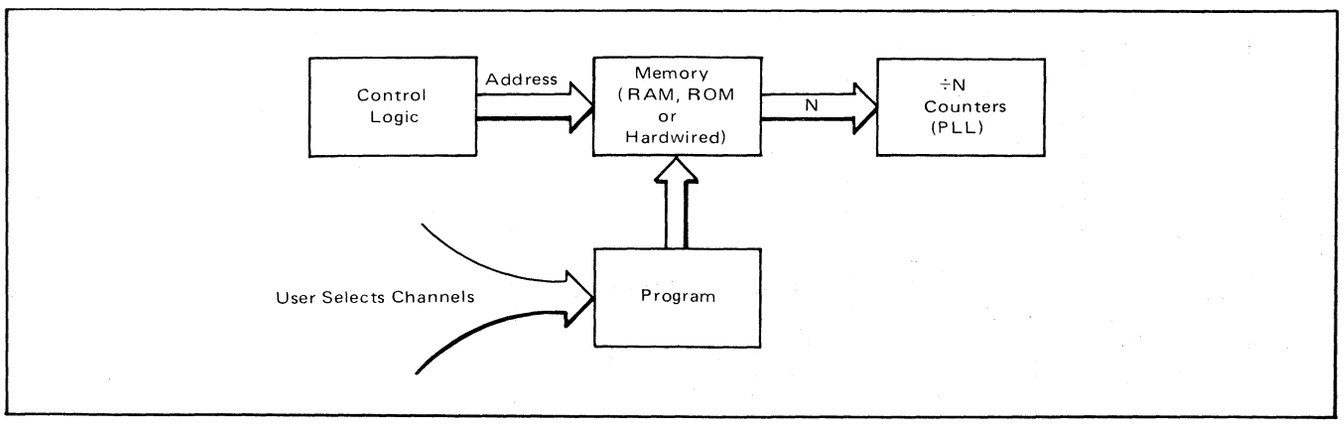

FIGURE 8 – A Phase-Locked Loop Scanner Logic Block Diagram

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